



UNITED STATES PATENT AND TRADEMARK OFFICE

*Pbn*  
UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,143	01/17/2002	Hirokazu Honda	NEC 00USFP553 DIV	9041

7590 11/05/2002  
Hayes Soloway  
175 Canal Street  
Manchester, NH 03101

EXAMINER

ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
----------	--------------

2827

DATE MAILED: 11/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/052,143

Applicant(s)

HONDA, HIROKAZU

Examiner

David A. Zarneke

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 13-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 January 2002 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☒ Certified copies of the priority documents have been received in Application No. 09/712105.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: .

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 13-15, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaji et al., US Patent 6,159,837.

Yamaji teaches a method of making a semiconductor device comprising:

providing a semiconductor substrate (1) having pads (2) thereon on which an insulating film (3) is formed through which the pads are exposed;

forming a wiring pattern (4) that extends over said insulating film and connects to said pads;

forming a stress relieving curable resin layer (5) [3, 20-49] on said wiring pattern and said insulating film, said stress relieving layer surrounding conductive sections (7) on lateral sides and connecting to said wiring pattern; and  
forming bumps (8) thereon (Figures).

Regarding claim 14, Yamaji teaches cutting the substrate into chips (8, 38+).

With respect to claim 15, Yamaji teaches forming the pads (2), forming a passivation film (3) with openings to said pads therein, and forming a second insulating film (9) on the passivation film (figure 4).

As to claims 21, Yamaji teaches a stress buffer layer made of a polyimide or epoxy based resin (3, 20+).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al., US Patent 6,159,837, as applied to claim 13 above.

Regarding claims 16 and 17, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the second insulating material to be a photosensitive material having a specific pyrolysis temperature (MPEP 2144.05(b)).

With respect to claim 18, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the conductive layer deposition layer method to be electrolysis plating (MPEP 2144.05(b)) and Yamaji teaches using patterning to form the wiring patterns ((5, 50+).

Regarding claim 20, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the elastic modulus or the stress buffer layer (MPEP 2144.05(b)).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al., US Patent 6,159,837, as applied to claim 13 above, and further in view of Takahashi et al., US Patent 6,153,448.

Yamaji, relied upon as taught above, fails to teach the forming of the conductive section first, then forming the stress buffer layer around it, and finally polishing the stress buffer layer such that the conductive sections are exposed.

Takahashi teaches a method of making a semiconductor device comprising:

forming conductive layers (11 and 31) on electrode pads (15) on the surface of a substrate (1);

depositing an insulating layer (32) over the entire surface; and

polishing the insulating layer such that the top surface of the conductive layers are exposed (figures 6A-6D).

It would have been obvious to one of ordinary skill in the art at the time of the invention to forming technique of Takahashi in the invention of Yamaji because the technique of Takahashi is an equivalent method that is more than well known in the art.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al., US Patent 6,159,837, as applied to claim 13 above, and further in view of Takahashi et al., US Patent 6,153,448, and Kim et al., US Patent 4,751,349.

Yamaji, relied upon as taught above, while teaching the use of a dual layer stress buffer layer (Figure 6), fails to teach the use of a dual layered conductive section formed in the manner claimed.

Takahashi teaches a method of making a semiconductor device comprising:

- forming conductive layers (11 and 31) on electrode pads (15) on the surface of a substrate (1);
- depositing an insulating layer (32) over the entire surface; and
- polishing the insulating layer such that the top surface of the conductive layers are exposed (figures 6A-6D).

It would have been obvious to one of ordinary skill in the art at the time of the invention to forming technique of Takahashi in the invention of Yamaji because the technique of Takahashi is an equivalent method that is more than well known in the art.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16

Art Unit: 2827

USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Kim recites a multi-layer metallic structure comprising:

- a) forming a polyimide layer (36) upon a substrate (10) with openings therein formed over vias (14 & 16);
  - b) forming capture pads (26) within the openings;
  - c) forming another polyimide layer (37) over the entire surface with openings therein;
  - d) forming inter-chip wiring (27) within the openings;
  - e) repeating c) and d);
- forming solder balls (32) on top of the last layer; and
- attaching a chip (31) to the solder balls.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the multiple insulating and conductive layers (redistribution layers) of Kim in the invention of Yamaji because the use of redistribution layers is commonly known equivalent technique for forming metallization layers.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Regarding claims 23, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the elastic modulus of the buffer layer (MPEP 2144.05(b)).

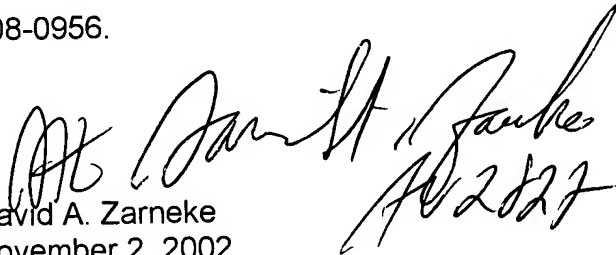
With respect to claims 24, Yamaji teaches a stress buffer layer made of a polyimide or epoxy based resin (3, 20+).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-7722 for regular communications and (703)-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

  
David A. Zarneke  
November 2, 2002